Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A detector arrangement with a plurality of detector elements ~~or image pixels, which~~, each of the plurality of detector elements ~~have~~ includes an integrated SD modulator, wherein for each detector element both the detector element and the corresponding integrated SD modulator reside on a same CMOS semiconductor structure and ~~, wherein~~ the SD modulator has a differential design and/~~or~~ a plurality of stages.

2. (Currently Amended) [[A]] The detector arrangement as claimed in claim 1, wherein the SD modulator is extended with a decimation filter to a SD- A/D converter.

3. Cancelled.

4. (Currently Amended) [[A]] The detector arrangement as claimed in claim 1, wherein the SD modulator for at least one of the plurality of detector elements has a current feedback on the signal of the at least one of the plurality of detector element with an SC current source.

5. (Currently Amended) [[A]] The detector arrangement as claimed in claim 1, wherein a cascaded arrangement of SD modulators in at least one detector element ~~or image pixel~~ is provided.

6. (Currently Amended) [[A]] The detector arrangement as claimed in claim 1, wherein the SD modulator has an Auto- Zero- Comparator.

7. (Original) A semiconductor-based image sensor with a detector arrangement as claimed in claim 1.

8. (Original) An X-ray detector with a detector arrangement as claimed in claim 1.

9. (Original) An X-ray apparatus, particularly for computer tomography, with a detector arrangement as claimed in claim 1.

10. (New) A radiation sensitive detector array, comprising:

a photosensor; and

a Sigma Delta Analog-to-Digital component; wherein the photosensor and the Sigma Delta Analog-to-Digital component are located on a same substrate.

11. (New) The radiation sensitive detector array of claims 10, wherein the Sigma Delta Analog-to-Digital component includes an integrator bank and a comparator.

12. (New) The radiation sensitive detector array of claims 11, wherein the integrator bank include two or more integrators.

13. (New) The radiation sensitive detector array of claims 12, wherein two or more integrators are different order integrators.

14. (New) The radiation sensitive detector array of claims 10, further including a decimation filter that produces a signal with a relatively lower sampling rate and a relatively higher dynamic range with respect to the output signal of the Sigma Delta Analog-to-Digital component and based on the output signal of the Sigma Delta Analog-to-Digital component.

15. (New) The radiation sensitive detector array of claims 14, wherein the decimation filter converts a one (1) bit data stream from the Sigma Delta Analog-to-Digital component into a seventeen (17) bit data signal.

16. (New) The radiation sensitive detector array of claims 14, wherein the decimation filter converts differential one (1) bit data streams from the Sigma Delta Analog-to-Digital component into a single seventeen (17) bit data signal.

17. (New) A method, comprising:

detecting radiation with a first component;

producing a first signal indicative of the detected radiation, wherein the first signal has a first dynamic range; and

generating a second signal, based on the first signal, with a second component; wherein the second signal has a second dynamic range, wherein the second dynamic range is greater than the first dynamic range, and the first and second components reside on a same integrated chip.

18. (New) The method of claim 17, wherein the first signal has a first sampling rate and the second signal has a second sampling rate, which is less than the first sampling rate.

19. (New) The method of claim 17, wherein the first component includes a photodetector and the second component includes a Sigma Delta modulator.

20. (New) The method of claim 17, wherein the first component includes a photodetector and the second component includes a Sigma Delta Analog-to-Digital converter.

21. (New) The method of claim 17, further including continuously integrating the first signal and generating the second signal based thereon.